DATA SHEET

TDA1593
IF amplifier/demodulator for FM car radio receivers

Product specification
Supersedes data of 1995 May 29
File under Integrated Circuits, IC01

1996 Oct 10

Philips Semiconductors

PHILIPS

FEATURES

- Balanced limiting amplifier
- Balanced coincidence demodulator
- Two open-collector stop pulse outputs for microcomputer tuning control
- Simulated behaviour of ratio detector (internal field strength and detuning dependent voltage for dynamic AF signal muting)
- Mono/stereo blend field strength indication control voltage
- AFC output
- Internal compensation of AF signal total harmonic distortion (THD)
- Built-in hum and ripple rejection circuits.

GENERAL DESCRIPTION

The TDA1593 provides IF amplification, symmetrical quadrature demodulation and level detection for quality FM car radio receivers and is suitable for mono and stereo reception. It may also be applied to common front ends, stereo decoders and AM receivers circuits.

All pin numbers mentioned in this data sheet refer to the SO-version (TDA1593T) unless otherwise specified.

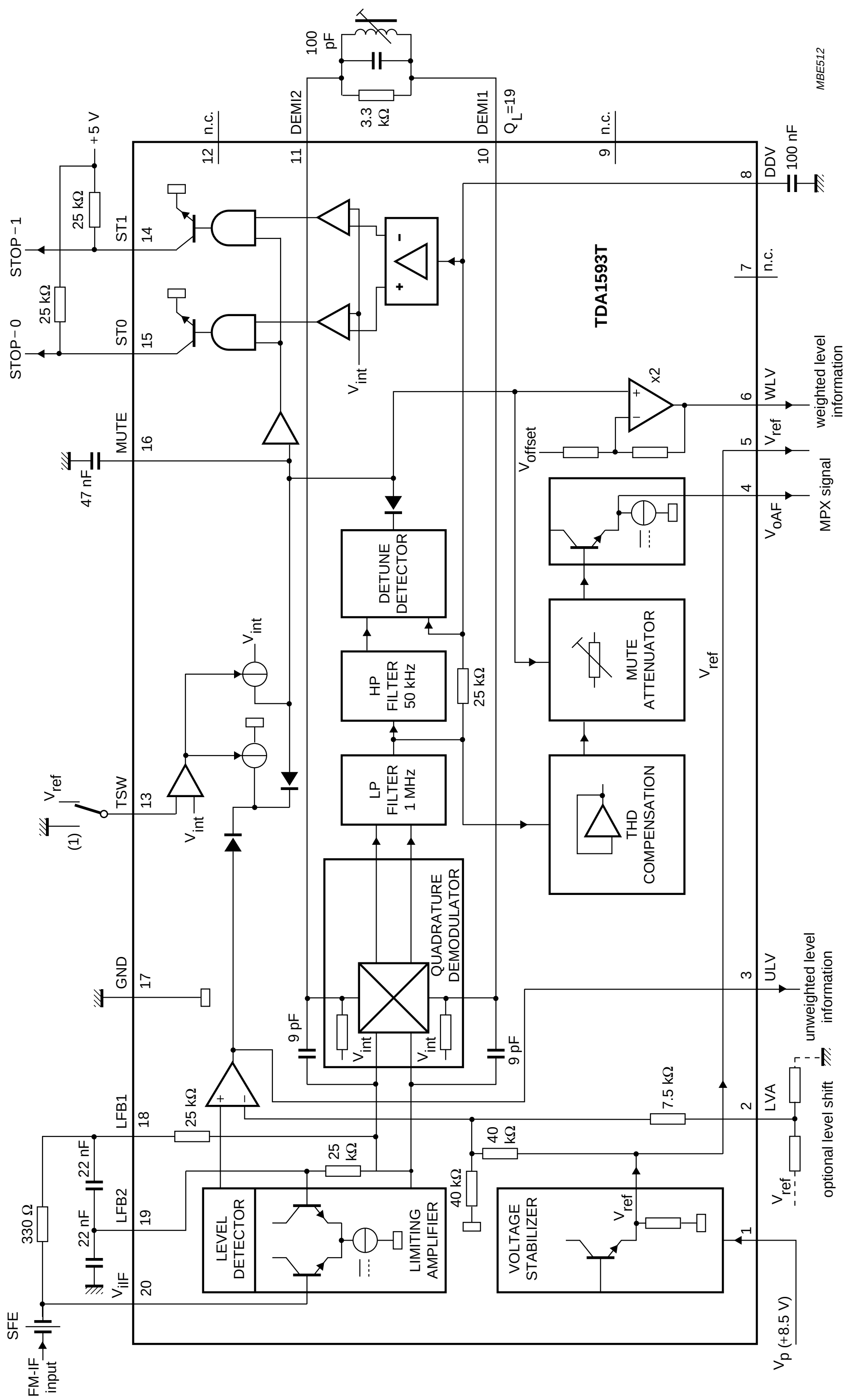
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 1)	7.5	8.5	12	V
I_P	supply current (I_2 = 0)	–	20	26	mA
V_{iIF}	IF input sensitivity for limiting on pin 20 (RMS value)	14	22	35	μV
V_{oAF}	AF output signal on pin 4 (RMS value)	180	200	220	mV
S/N	signal-to-noise ratio (f_m = 400 Hz; Δf = ±75 kHz)	–	82	–	dB
THD	total harmonic distortion (f_m = 1 kHz; Δf = ±75 kHz)	–	0.2	0.6	%
T_{amb}	operating ambient temperature	–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1593	DIP18	plastic dual in-line package; 18 leads (300 mil)	SOT102-1
TDA1593T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM



(1) Connecting pin 13 to ground is only allowed to measure the current on pin 16; it is not used in application.

Fig.1 Block diagram and application circuit.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT102-1 DIP18	SOT163-1 SO20	
V_P	1	1	supply voltage (+8.5 V)
LVA	2	2	level adjustment for stop condition
ULV	3	3	unweighted level output
V_{oAF}	4	4	audio frequency output (MPX signal)
V_{ref}	5	5	reference voltage output
WLV	6	6	weighted level output
n.c.	7	7	not connected
DDV	8	8	detune detector voltage
n.c.	–	9	not connected
DEMI1	9	10	demodulator input 1
DEMI2	10	11	demodulator input 2
n.c.	–	12	not connected
TSW	11	13	tau switch input
ST1	12	14	STOP-1, stop pulse output 1
ST0	13	15	STOP-0, stop pulse output 0
MUTE	14	16	muting voltage
GND	15	17	ground (0 V)
LFB1	16	18	IF limiter feedback 1
LFB2	17	19	IF limiter feedback 2
V_{iIF}	18	20	IF signal input

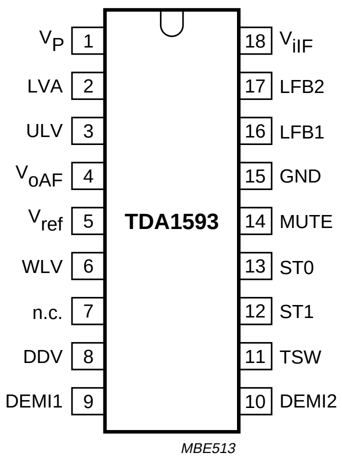


Fig.2 Pin configuration for DIP-version.

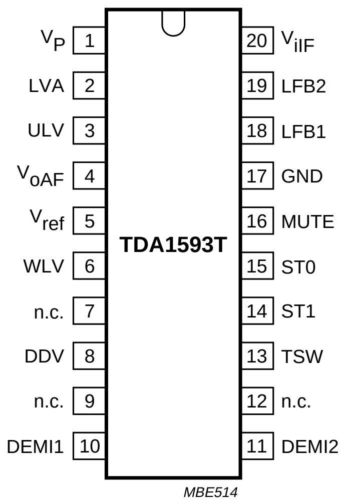


Fig.3 Pin configuration for SO-version.

FUNCTIONAL DESCRIPTION

The limiter amplifier has five stages of IF amplification using balanced differential limiter amplifiers with emitter follower coupling.

Decoupling of the stages from the supply voltage line and an internal high-ohmic DC feedback loop give a very stable IF performance. The amplifier gain is virtually independent of changes in temperature.

The FM demodulator is fully balanced and compromises two cross-coupled differential amplifiers.

The quadrature detection of the FM signal is performed by direct feeding of one differential amplifier from the limiter amplifier output, and the other via an external 90 degrees phase shifting network. The demodulator has a good stability and a small zero-cross-over shift. The bandwidth of the demodulator output is restricted by an internal low-pass filter to approximately 1 MHz. Non-linearities, which are introduced by demodulation, are compensated by the THD compensation circuit. For this reason, the demodulator resonance circuit (between pins 10 and 11) must have a loaded Q-factor of 19. Consequently, there is no need for the demodulator tuned circuit to be adjusted for minimum distortion. Adjustment criterion is a symmetrical stop pulse. The control voltage for the mute attenuator (pin 16) is derived from the values of the level detector and the detuning detector output signals.
The mute attenuator has a fast attack and a slow decay determined by the capacitor on pin 16. The AF signal is fed via the mute attenuator to the output (pin 4). A weighted control voltage (pin 6) is obtained from the mute attenuator control voltage via a buffer amplifier that introduces an additional voltage shift and gain.

The level detector generates a voltage output signal proportional to the amplitude of the input signal.
The unweighted level detector output signal is available.
The open-collector tuning stop output voltages STOP-0 and STOP-1 (pins 15 and 14) are derived from the detuning and the input signal level. The pins 14 and 15 may be tied together, if only one tuning-stop output is required.

LIMITING VALUES

TDA1593T pinning

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	–0.3	+13	V
V_n	voltage at pins 2, 4, 5, 6, 10, 11 and 16	–0.3	+10	V
	voltage at pins 3, 8, 14, 15, 18, 19 and 20	–0.3	V_P	V
V_{13}	voltage on pin 13	–	6	V
$I_{14, 15}$	current at pins 14 and 15	–	2	mA
P_{tot}	total power dissipation	–	360	mW
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	–40	+85	°C
V_{es}	electrostatic handling; note 1			
	all pins except pin 5	–2000	+2000	V
	pin 5	–2000	+800	V

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT102-1	80	K/W
	SOT163-1	90	K/W

CHARACTERISTICS

V_P = 8.5 V; T_{amb} = +25 °C; f_{IF} = 10.7 MHz; deviation ±22.5 kHz with f_m = 400 Hz; V_i = 10 mV (RMS) at pin 20; de-emphasis of 50 µs; tuned circuit at pins 10 and 11 aligned for symmetrical stop pulses; measurements taken in Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MIN.	UNIT
V_P	supply voltage (pin 1)		7.5	8.5	12	V
I_P	supply current	I_2 = 0	–	20	26	mA
IF amplifier and demodulator						
Z_i	demodulator input impedance between pins 10 and 11		25	40	55	kΩ
C_i	demodulator input capacitance between pins 10 and 11		–	6	–	pF
AF output (pin 4)						
R_o	output resistance		–	400	–	Ω
V_4	DC output level	V_{iIF} ≤ 5 µV (RMS) on pin 20	2.75	3.1	3.45	V
PSRR	power supply ripple rejection (pin 4)	f = 1000 Hz; V_{ripple} = 50 mV (RMS)	33	36	–	dB
Tuning stop detector						
Δf_{STOP-0}	detuning frequency for STOP-0 (pin 15)	see Fig.9 V_{15} ≥ 3.5 V V_{15} ≤ 0.3 V	 – +22.0	 – –	 +14.0 –	 kHz kHz
Δf_{STOP-1}	detuning frequency for STOP-1 (pin 14)	see Fig.8 V_{14} ≥ 3.5 V V_{14} ≤ 0.3 V	 – –22.0	 – –	 –14.0 –	 kHz kHz
V_{20}	dependency on input voltage for STOP-0 and STOP-1 (RMS value)	see Fig.7 $V_{14, 15}$ ≥ 3.5 V $V_{14, 15}$ ≤ 0.3 V	 250 –	 – –	 – 50	 µV µV
$V_{14, 15}$	output voltage	$I_{14, 15}$ = 1 mA	–	–	0.3	V
Reference voltage source (pin 5)						
V_{ref}	reference output voltage	I_5 = –1 mA	3.3	3.7	4.1	V
R_5	output resistance	I_5 = –1 mA	–	40	80	Ω
TC	temperature coefficient		–	3.3	–	mV/K
External muting						
V_{16}	muting voltage at I_2 = 0	V_{20} ≤ 5 µV (RMS); see Fig.10	1.45	1.75	2.05	V
		V_{20} = 1 mV (RMS)	3.0	3.45	3.9	V
S	steepness of control voltage	slope: 100 µV ≤ V_{20} ≤ 100 mV; 20 Δlog V_{20} = 20 dB $\left(\frac{\Delta V_{16}}{\Delta \log V_{20}}\right)$	–	0.85	–	V/dec

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MIN.	UNIT
Internal mute α**;** note 1						
α	mute voltage	$V_{16} \geq V_{ref}$	–	0	–	dB
		$V_{16} = 0.77V_{ref}$	1.5	–	4.5	dB
		$V_{16} = 0.55V_{ref}$	–	20	–	dB
I_{16}	current for capacitor (pin 16)					
	charge current	$V_{13} = 0$ V	–	–8	–	μA
	discharge current	$V_{13} = 0$ V	–	+120	–	μA
	charge current	$V_{13} = V_{ref}$	–	–100	–	μA
	discharge current	$V_{13} = V_{ref}$	–	+120	–	μA
Level detector						
R_6	output resistance		–	–	500	Ω
V_6	output voltage at $I_2 = 0$	$V_{20} \leq 5$ μV (RMS); see Fig.11	0.1	–	1.1	V
		$V_{20} = 1$ mV (RMS)	3.0	–	4.2	V
		±200 kHz detuning	1.2	1.5	1.8	V
ΔV_6	output voltage at detuning	±45 kHz detuning	–	–	0.2	V
TC	temperature coefficient		–	3.3	–	mV/K
S	steepness of control voltage	slope: 50 μV ≤ V_{20} ≤ 50 mV; 20 Δlog V_{20} = 20 dB $\left(\frac{\Delta V_6}{\Delta \log V_{20}}\right)$	1.4	1.7	2.0	V/dec
$\Delta V_6/\Delta f$	slope of output voltage at detuning	Δf = 125 ±20 kHz	–	35	–	mV/kHz
S	level shift adjustments					
	range by pin 2	$\pm\Delta V_6/V_{ref}$	0.42	0.5	–	V/V
	gain	$-\Delta V_6/\Delta V_2$	–	1.7	–	V/V
	range by pin 2	$\pm\Delta V_{16}/V_{ref}$	0.21	0.25	–	V/V
	gain	$-\Delta V_{16}/\Delta V_2$	–	0.85	–	V/V

Note

1. $\alpha = 20 \log \frac{\Delta V_{4(FM-MUTE-OFF)}}{\Delta V_{4(FM-MUTE-ON)}}$

OPERATING CHARACTERISTICS

V_P = 7.5 to 12 V; T_{amb} = +25 °C; f_{IF} = 10.7 MHz; deviation ±22.5 kHz with f_m = 400 Hz; V_i = 10 mV (RMS) at pin 20; de-emphasis of 50 µs; tuned circuit at pins 10 and 11 aligned for symmetrical stop pulses; measurements taken in Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MIN.	UNIT
IF amplifier and demodulator						
V_i	input signal for start of limiting (–3 dB) (RMS value; pin 20)	V_{16} = 4.5 V	14	22	35	µV
	input signal for signal-to-noise ratio (RMS value)	f = 250 to 15000 Hz; V_{16} = 4.5 V				
		S/N = 26 dB	–	15	–	µV
		S/N = 46 dB	–	60	–	µV
S/N	signal-to-noise ratio	deviation ±75 kHz; f_m = 400 Hz	–	82	–	dB
V_o	AF output signal (RMS value; pin 4)		180	200	220	mV
THD	total harmonic distortion	deviation ±75 kHz; f_m = 1 kHz				
	without de-emphasis		–	0.2	0.6	%
	±25 kHz detuning		–	–	1.0	%
α_{AM}	AM suppression on pin 4	m = 30%; on pin 20				
	V_i = 0.3 to 1000 mV (RMS)		43	55	–	dB
	V_i = 1 to 300 mV (RMS)		57	65	–	dB
Tuning stop detector						
Δf_{STOP-0}	detuning frequency for STOP-0 (pin 15)	see Fig.9				
		$V_{15} \geq 3.5$ V	–	–	+14.0	kHz
		$V_{15} \leq 0.3$ V	+22.0	–	–	kHz
Δf_{STOP-1}	detuning frequency for STOP-1 (pin 14)	see Fig.8				
		$V_{14} \geq 3.5$ V	–	–	–14.0	kHz
		$V_{14} \leq 0.3$ V	–22.0	–	–	kHz
V_{20}	dependence on input voltage for STOP-0 and STOP-1 (RMS value)	see Fig.7				
		$V_{14, 15} \geq 3.5$ V	250	–	–	µV
		$V_{14, 15} \leq 0.3$ V	–	–	50	µV
R_8	internal low-pass resistance of detune detector		12	25	50	kΩ
V_8	voltage on capacitor	$V_i \leq 5$ µV (RMS) on input pin 20	–	2.2	–	V
Level detector (I_2 = 0)						
V_6	output voltage	$V_{20} \leq 5$ µV (RMS)	0.1	–	1.1	V
		V_{20} = 1 mV (RMS)	3.0	–	4.2	V
Reference voltage source (pin 5)						
V_{ref}	reference output voltage	I_5 = –1 mA	3.3	3.7	4.1	V

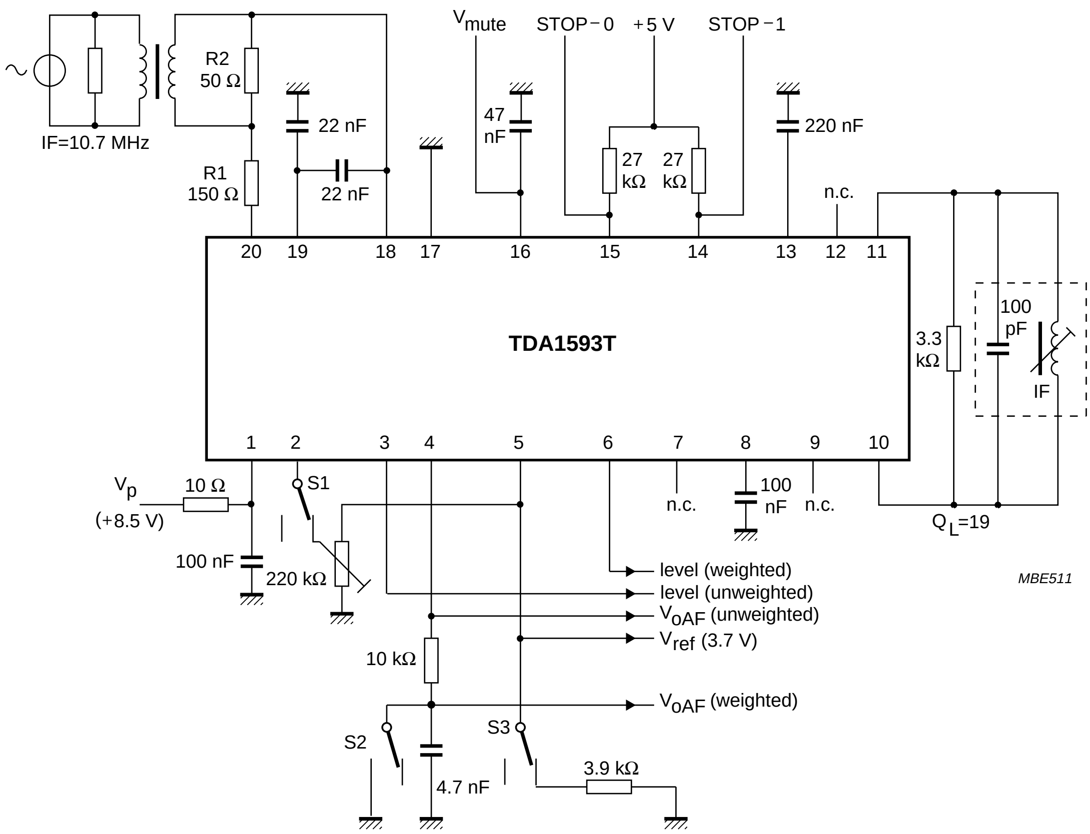
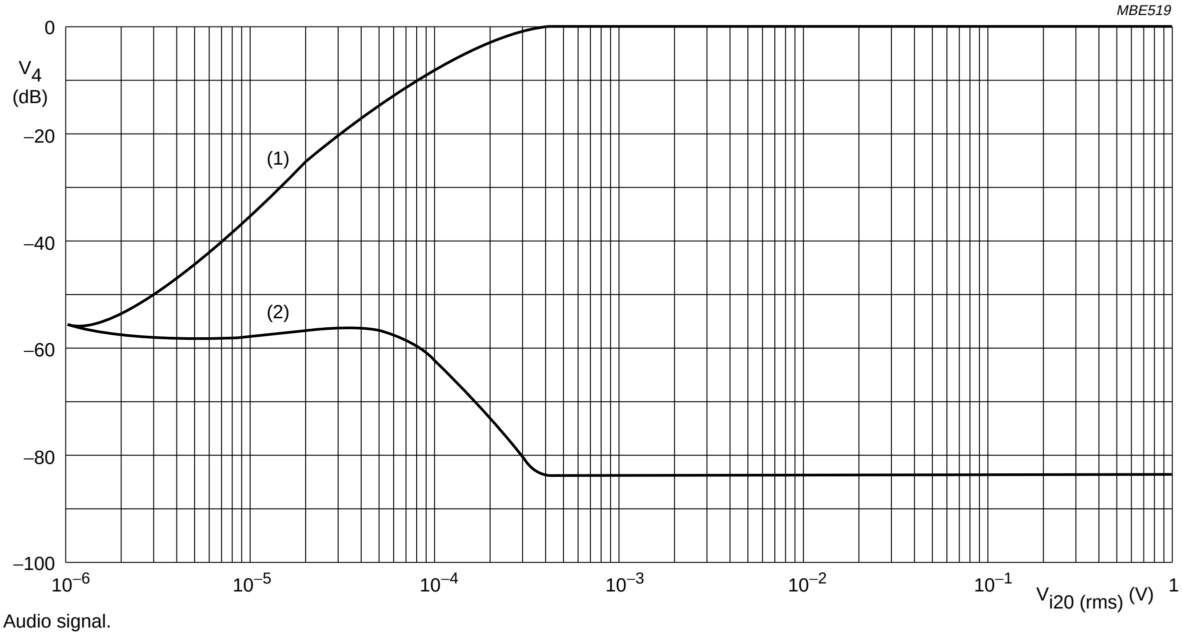


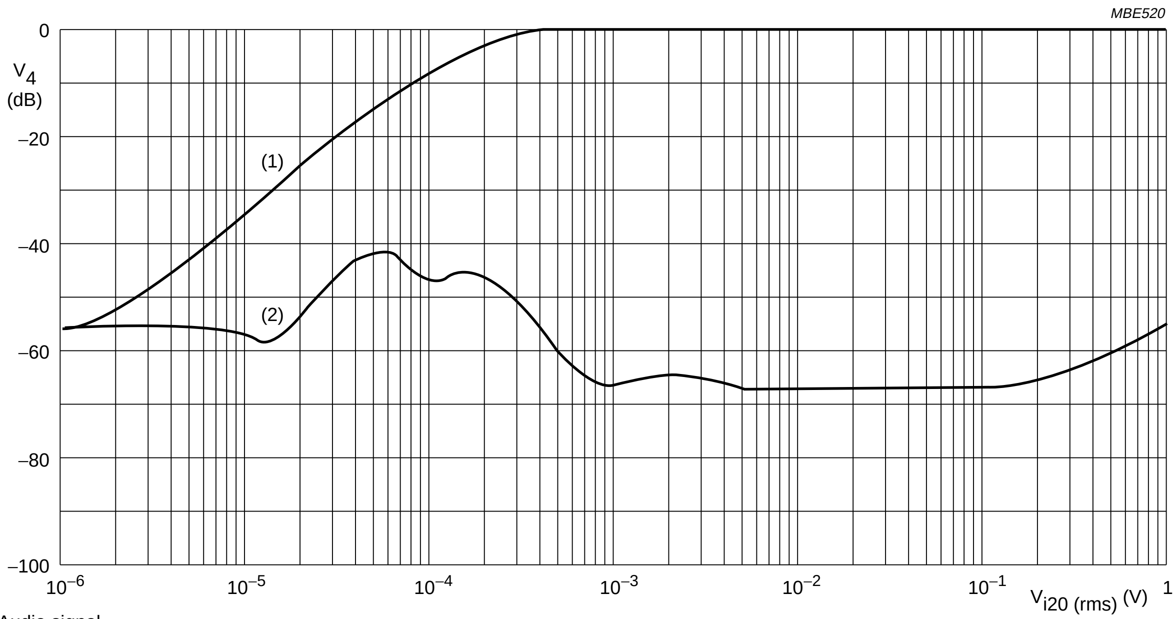
Fig.4 Test circuit.



(1) Audio signal.

(2) Noise.

Fig.5 Audio signal and noise as functions of the input signal V_{iIF} (pin 20) with Δf = ±22.5 kHz; f_m = 1 kHz; de-emphasis 50 μs.



(1) Audio signal.

(2) Spurious AM signal.

Fig.6 Typical AM suppression as a function of the input signal V_{iIF} (pin 20) with Δf = ±22.5 kHz; f_m = 1 kHz; AM with f_m = 400 Hz; m = 0.3 and 250 to 15000 Hz bandwidth.

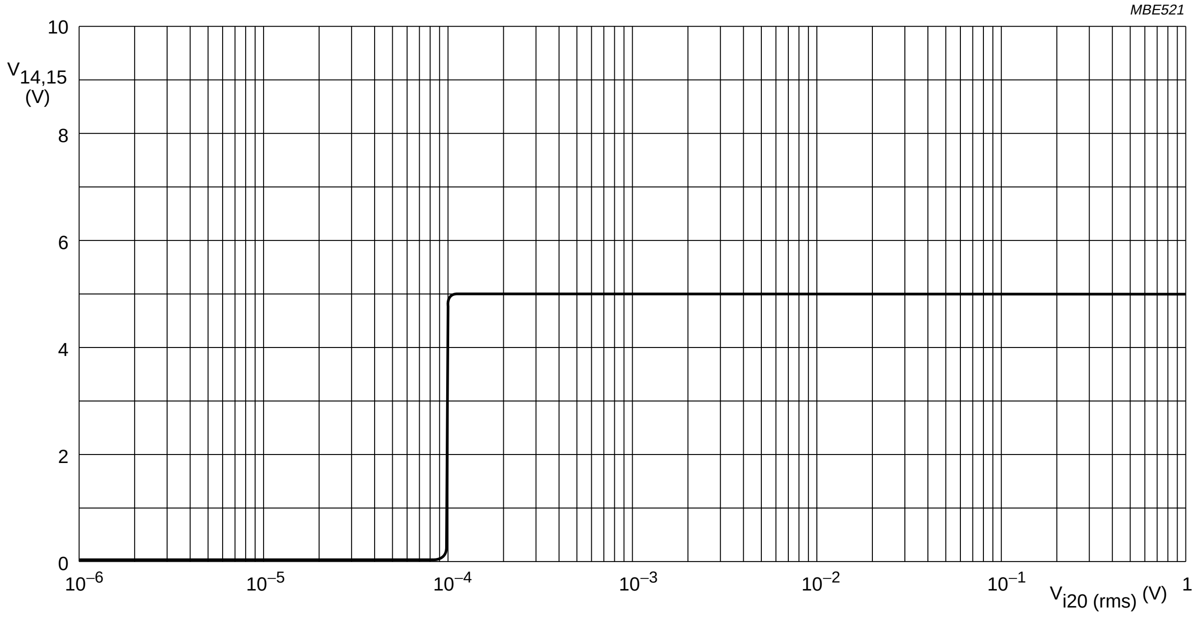


Fig.7 STOP-0 and STOP-1 output voltage dependent on input signal V_{iIF} (pin 20).

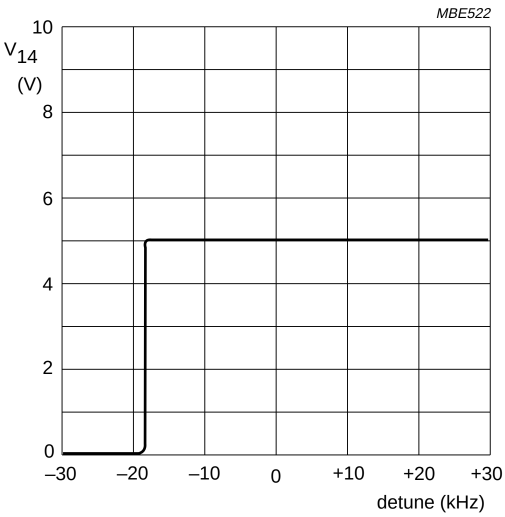


Fig.8 STOP-1 output voltage dependent on V_{iIF} = 10 mV (RMS) (pin 20).

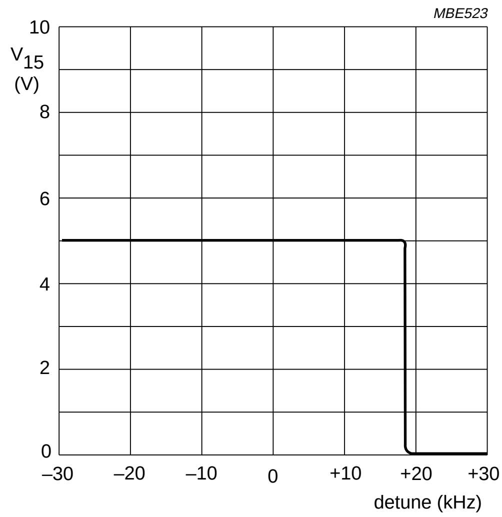
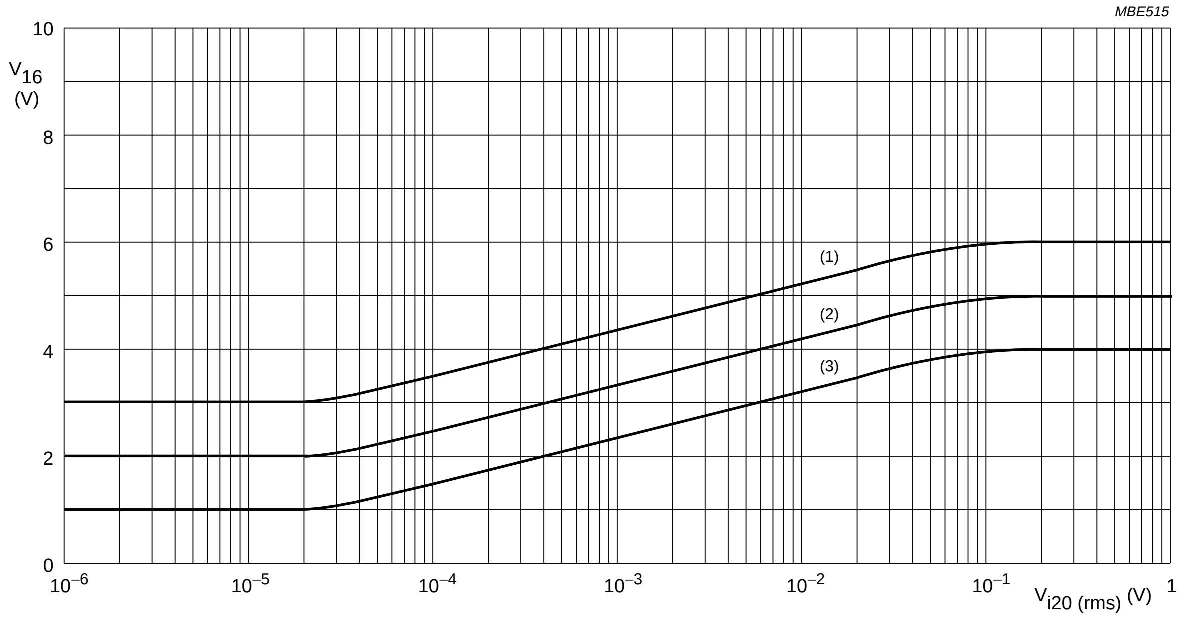
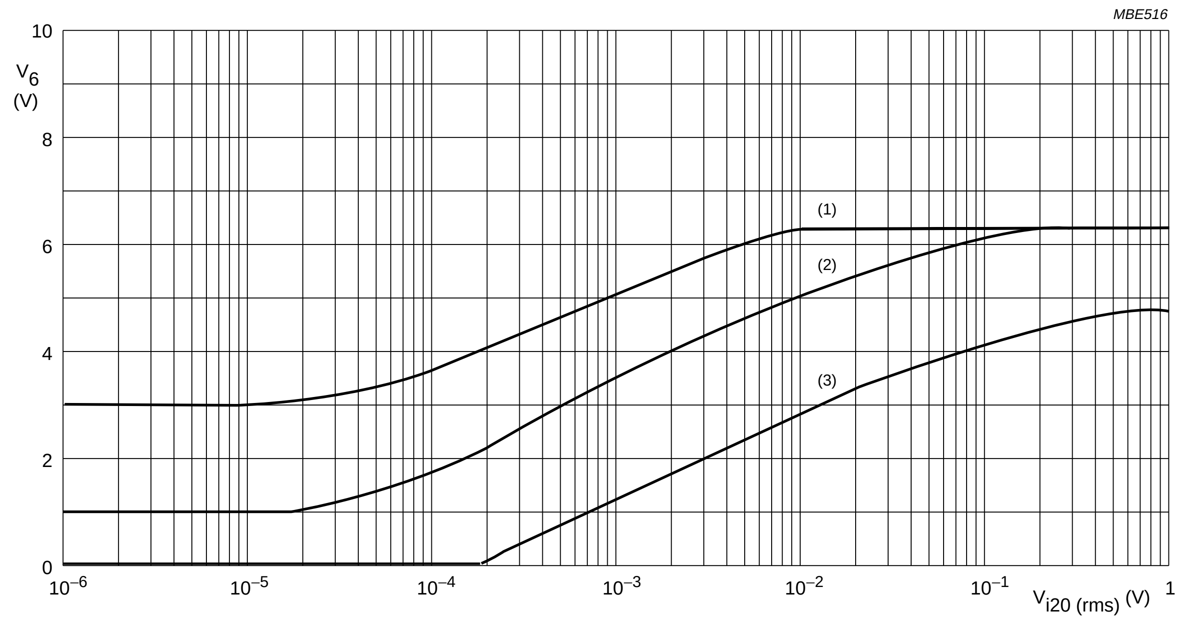


Fig.9 STOP-0 output voltage dependent on V_{iIF} = 10 mV (RMS) (pin 20).



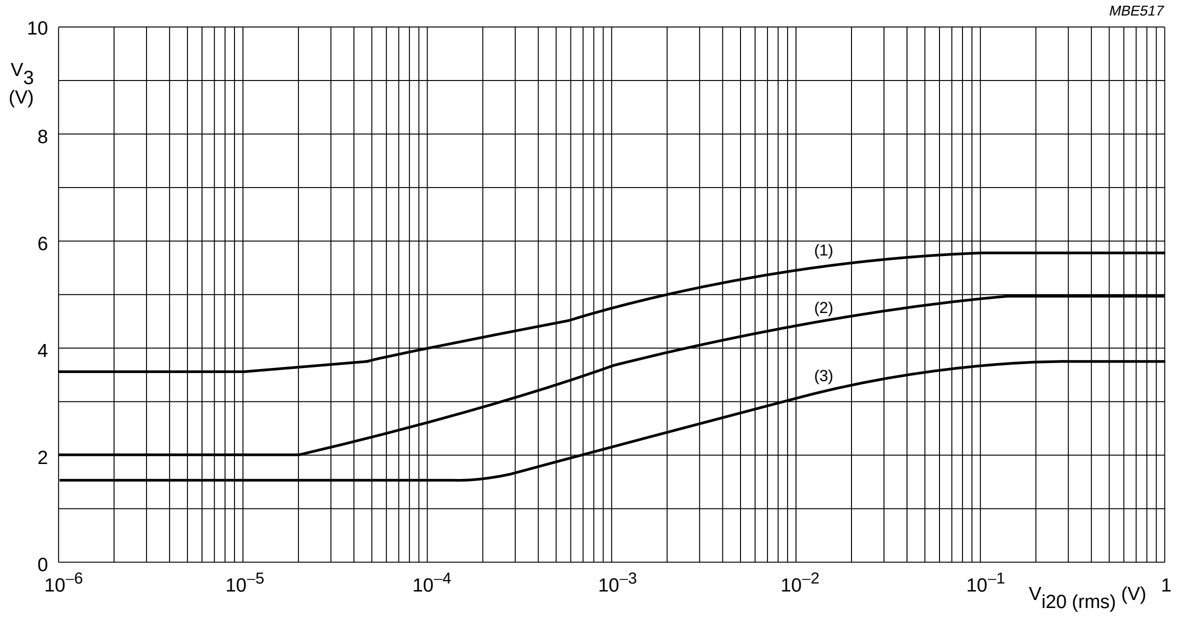
(1) V_2 = 0 V.
(2) I_2 = 0 mA.
(3) $V_2 = V_{ref}$.

Fig.10 External mute voltage V_{16} dependent on input signal V_{iIF} (pin 20); typical adjusting range.



(1) V_2 = 0 V.
(2) I_2 = 0 mA.
(3) $V_2 = V_{ref}$.

Fig.11 Control voltage V_6 dependent on input signal V_{iIF} (pin 20); typical adjusting range.



(1) V_2 = 0 V.
(2) I_2 = 0 mA.
(3) $V_2 = V_{ref}$.

Fig.12 Level output voltage V_3 dependent on input signal V_{iIF} (pin 20); typical adjusting range.

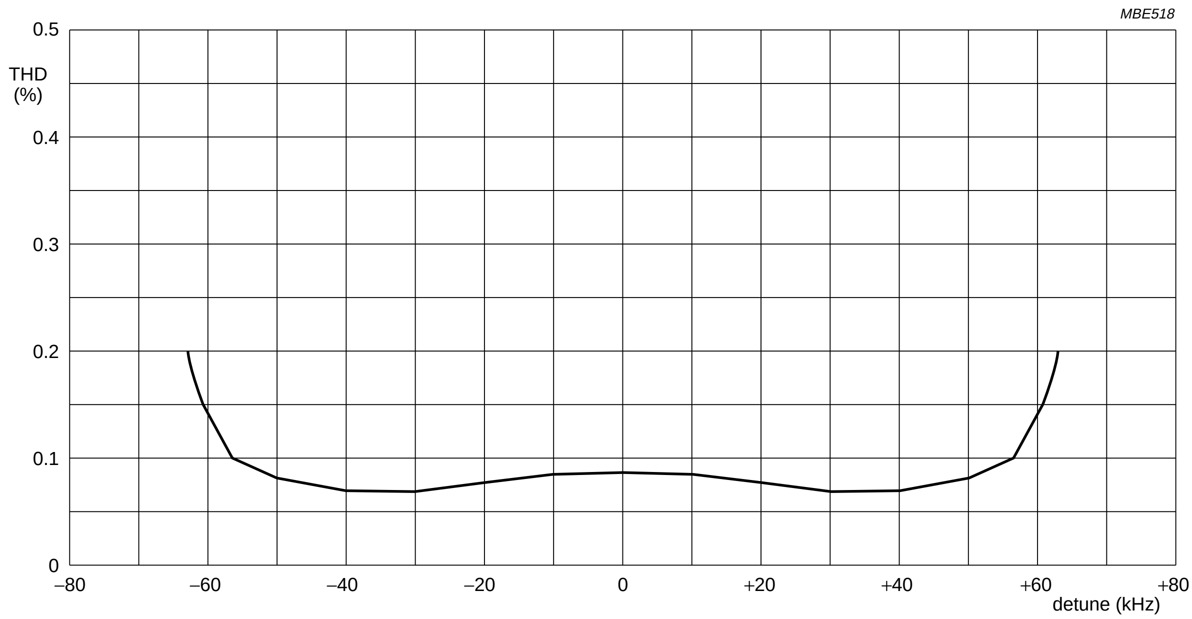
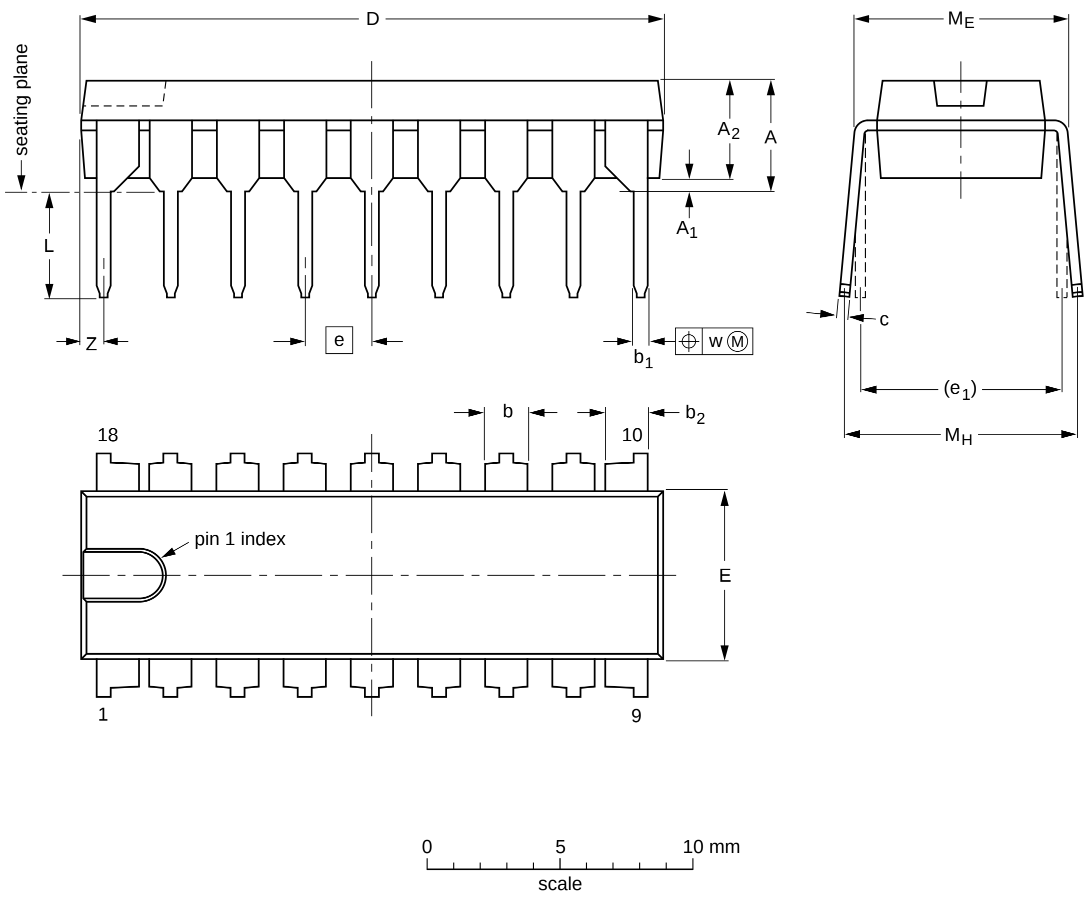


Fig.13 Total harmonic distortion dependent on detuning; $\Delta f = \pm75$ kHz; f_m = 1 kHz; V_{iIF} = 10 mV.

PACKAGE OUTLINES

DIP18: plastic dual in-line package; 18 leads (300 mil) SOT102-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

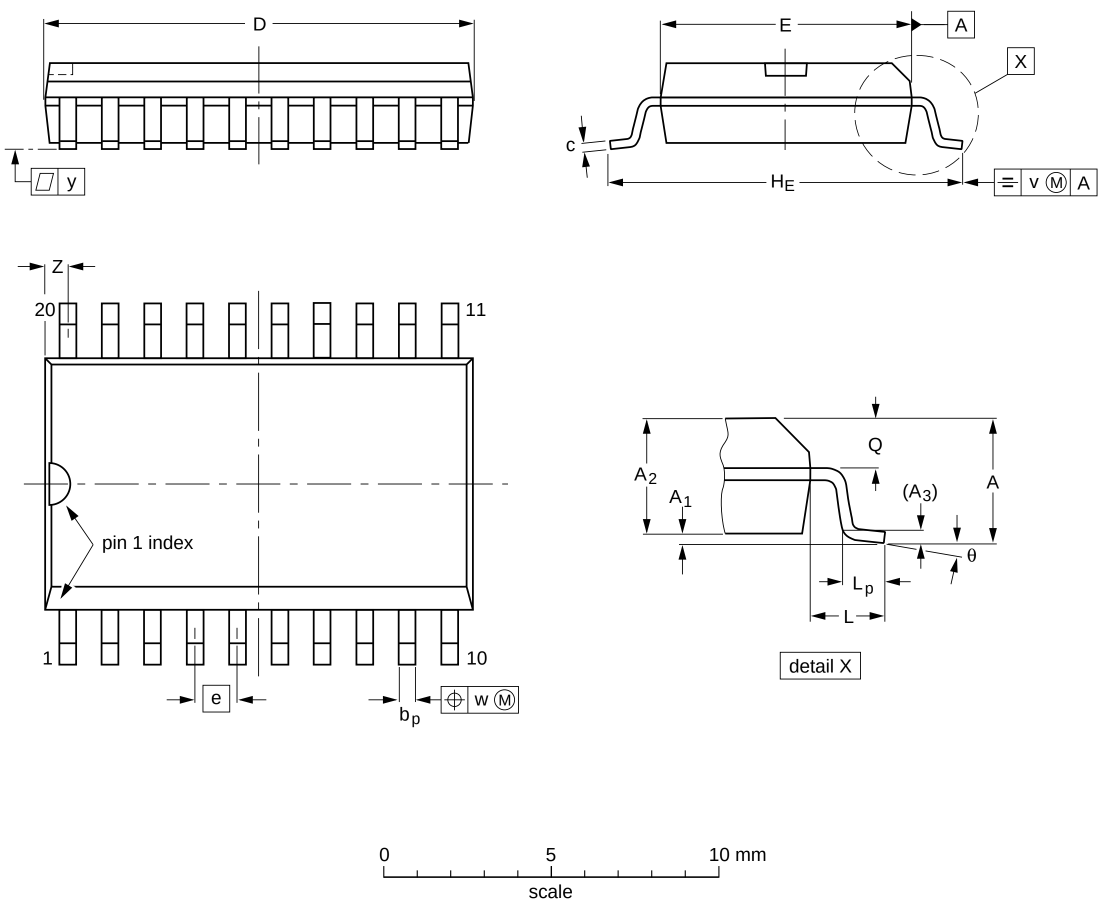
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D [(1)]	E [(1)]	e	e_1	L	M_E	M_H	w	Z [(1)] max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	1.40 1.14	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	0.85
inches	0.19	0.020	0.15	0.055 0.044	0.021 0.015	0.055 0.044	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.033

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT102-1						~~93-10-14~~ 95-01-23

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic small outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

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